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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,648	06/24/2003	Pranay Ashar	A8612	1307

7590 06/30/2004

SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC  
 2100 Pennsylvania Avenue, N. W.  
 Washington, DC 20037-3202

EXAMINER

ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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# Office Action Summary

Application No.

10/601,648

Applicant(s)

ASHAR ET AL.

Examiner

Esaw T Abraham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

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## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 06/24/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Claim 6 is presented for examination.

\*\*\*\*\* The examiner considers the preliminary amendment (claims 1-5, 7 and 8 are canceled in the preliminary amendment) filed on 06/24/03.

#### *Priority*

2. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 119 (e) (provisional application # 60/142,537) filed on 07/07/1999.

#### *Information Disclosure Statement*

3. The examiner has been considered the references listed in the information disclosure statement submitted on 06/24/03 (see attached PTO-1449).

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsunaga** (U.S. PN: 5,909,374) in view of **Gupta et al.** (U.S. PN: 6,026,222).

As per claim 6, Matsunaga teaches or discloses a logic circuit verifying system and method for checking whether or not two combinational logic circuits having no internal states are equivalent with each other (see col. 1, lines 7-11). Matsunaga teaches a method for efficiently verifying the equivalence in function of two combinational logic circuits (see col. 3, lines 41-44). Further, Matsunaga teaches a logic circuit verifying system for use in an information processing system for verifying equivalence of two logic circuits and outputting a verification result comprising a signal line selecting means (multiplexing) for selecting and adding to the first set of signal lines, logical function generating means for generating logical functions of the signals and determining means for determining whether the two signal lines are equivalent from the generated logical functions (see claim 1). Furthermore, Matsunaga in figures 3 and 5 teaches a scheme where the error detection and equivalence verification involve the addition of external input and this includes disconnecting the original circuitry and reconstructing an additional logic unit to produce this "psuedo", or external input (see col. 4, lines 5-9). Matsunaga **does not explicitly** teach miter circuits used for combinational equivalence checking. **However**, Gupta et al. in an analogous art teach a system for checking the equivalence of combinational circuits (see col. 1, lines 7-14) and further in figure 1 Gupta et al. teach two generic circuits that are operated by an "XOR" circuit which represent the actual miter circuit and if the XOR outputs a zero, then

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the two circuits are equivalent. **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to modify Matsunaga's system by adding a miter circuit for equivalence checking. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because an XOR is cheap and simple in design to build a reliable, fast actual error site tester.

*Conclusion*

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


US PN: 5,831,996 Abramovici et al.

US PN: 6,086,626 Jain et al.

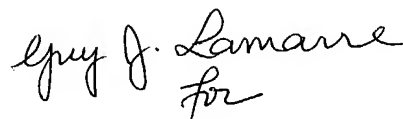
6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

  
Esaw Abraham

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for

Albert DeCady  
Primary Examiner

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